FIG. 1

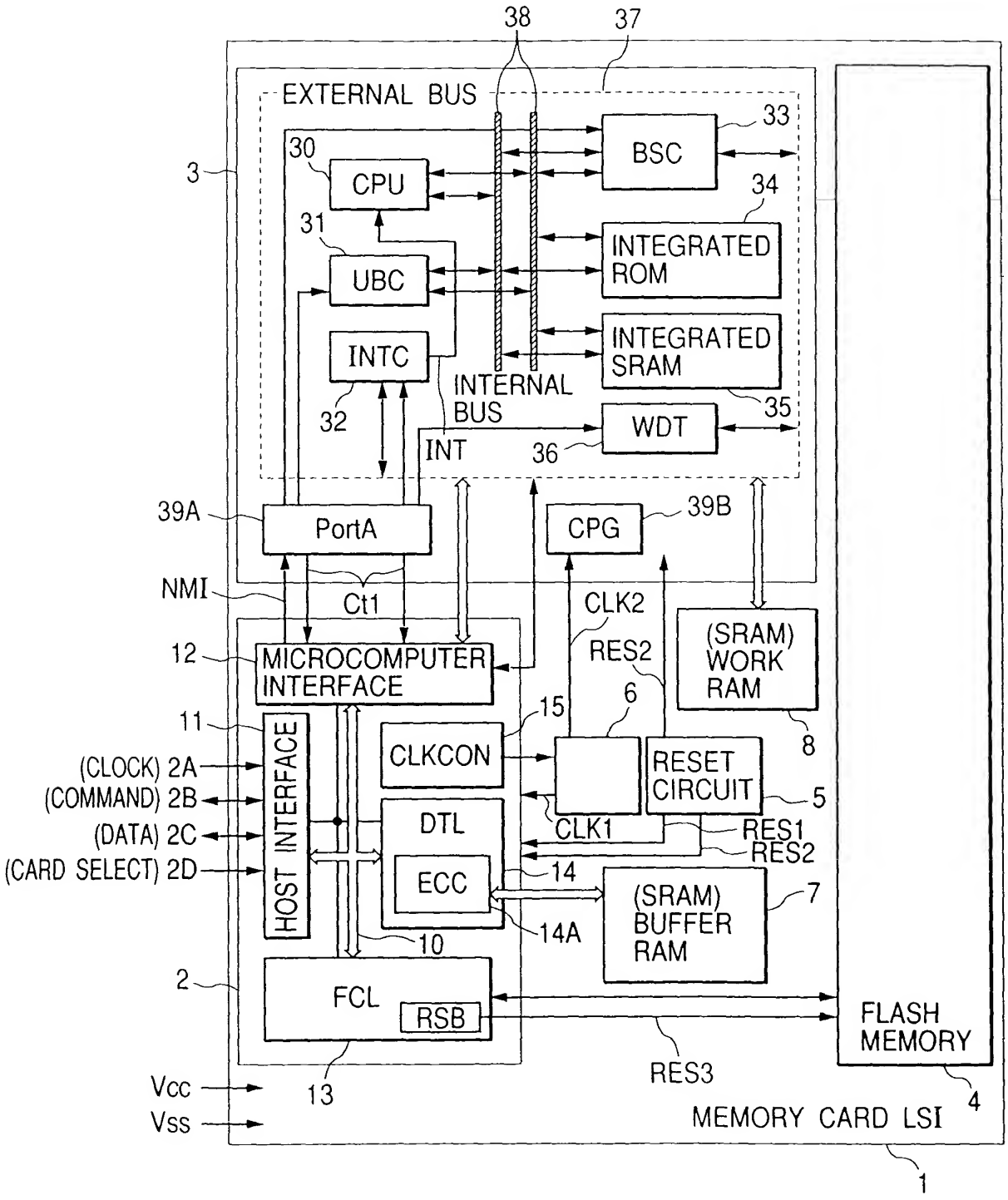
38
37
EXTERNAL BUS
33
BSC
30
CPU
3
34
INTEGRATED ROM
31
UBC
INTEGRATED SRAM
INTC
INTERNAL BUS
32
35
WDT
INT
36
39A
PortA
CPG
39B
NMI
Ct1
CLK2
(SRAM) WORK RAM
12
MICROCOMPUTER INTERFACE
RES2
6
11
15
CLKCON
RESET CIRCUIT
8
(CLOCK) 2A
(COMMAND) 2B
(DATA) 2C
(CARD SELECT) 2D
HOST INTERFACE
DTL
CLK1
RES1
RES2
5
ECC
14
7
(SRAM) BUFFER RAM
14A
10
2
FCL
RSB
FLASH MEMORY
RES3
Vcc
Vss
13
4
MEMORY CARD LSI
1

FIG. 2

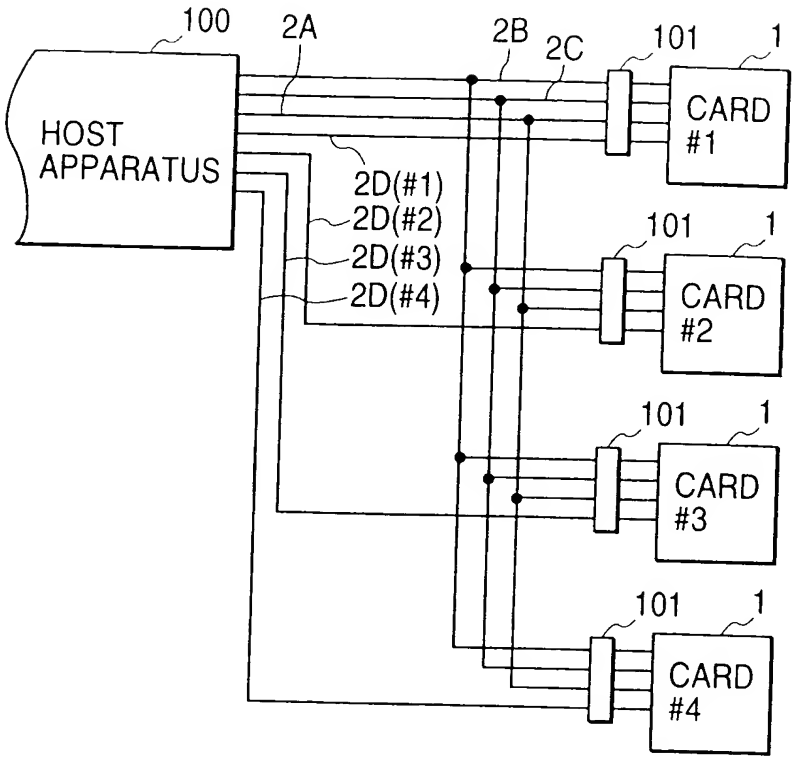
100
2A
2B
2C
101
1
HOST APPARATUS
CARD #1
2D(#1)
2D(#2)
2D(#3)
2D(#4)
CARD #2
CARD #3
CARD #4

FIG. 3

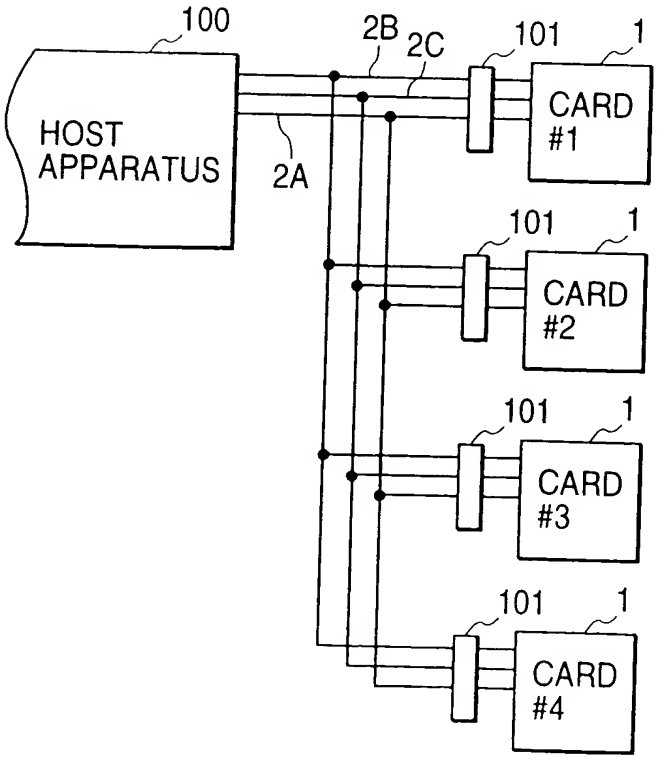
100
2B
2C
101
1
HOST APPARATUS
2A
CARD #1
CARD #2
CARD #3
CARD #4

FIG. 4

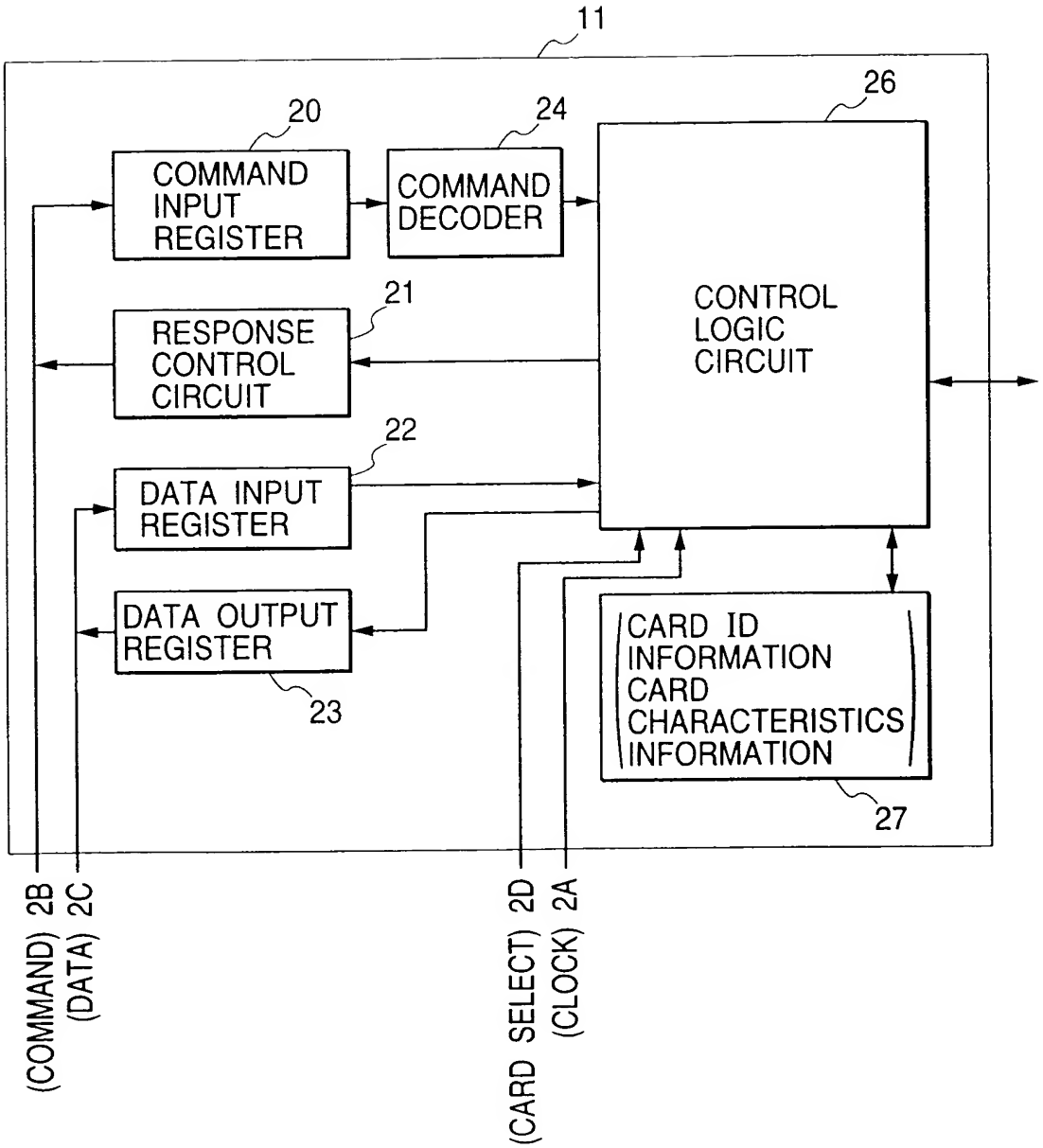
11
20
COMMAND INPUT REGISTER
24
COMMAND DECODER
26
CONTROL LOGIC CIRCUIT
21
RESPONSE CONTROL CIRCUIT
22
DATA INPUT REGISTER
DATA OUTPUT REGISTER
23
CARD ID INFORMATION
CARD CHARACTERISTICS INFORMATION
27
(COMMAND) 2B
(DATA) 2C
(CARD SELECT) 2D
(CLOCK) 2A

FIG. 5

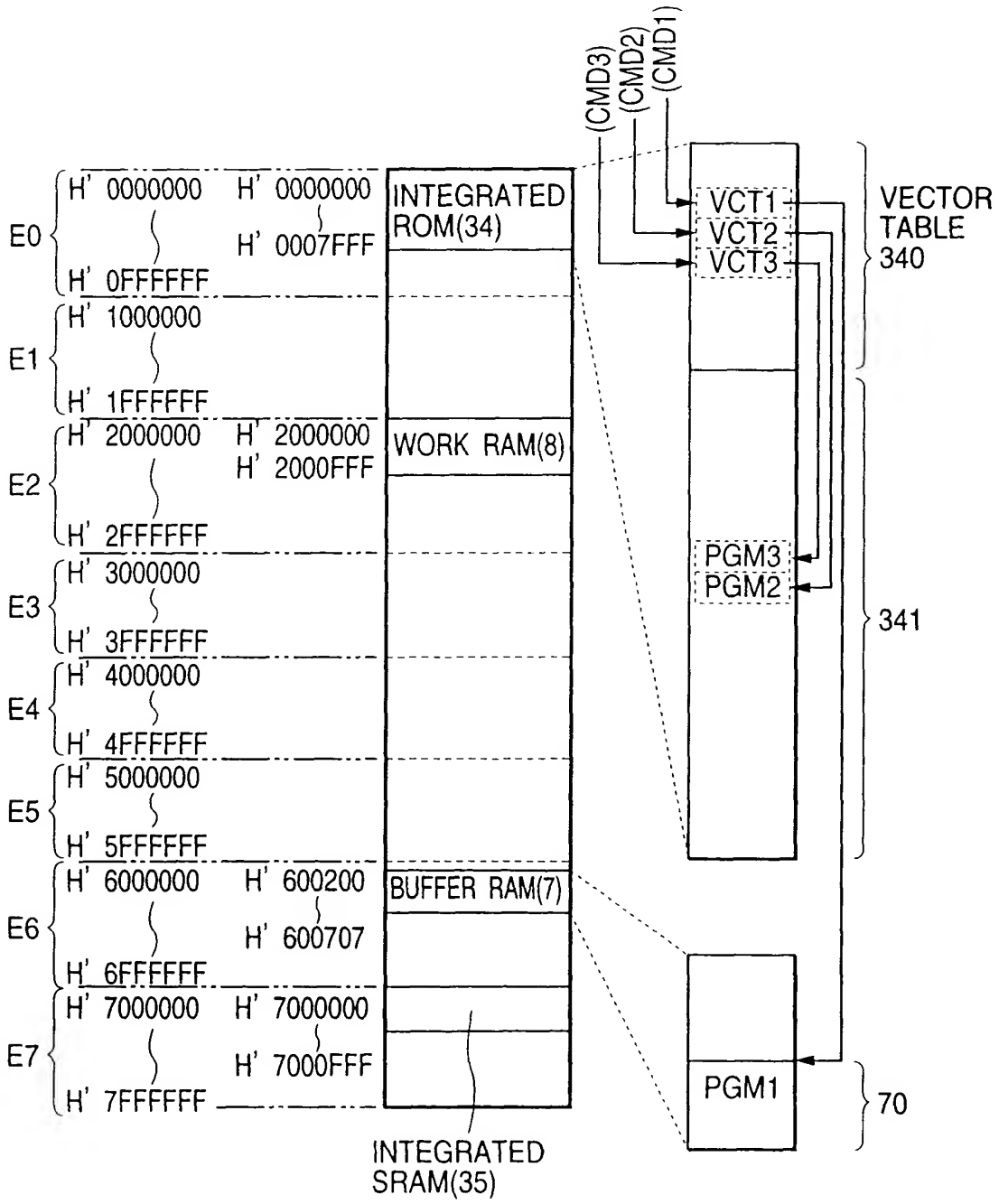
(CMD3)
(CMD2)
(CMD1)
E0
H' 0000000
H' 0000000
H' 0007FFF
H' 0FFFFFF
INTEGRATED ROM(34)
E1
H' 1000000
H' 1FFFFFF
E2
H' 2000000
H' 2000000
H' 2000FFF
H' 2FFFFFF
WORK RAM(8)
E3
H' 3000000
H' 3FFFFFF
E4
H' 4000000
H' 4FFFFFF
E5
H' 5000000
H' 5FFFFFF
E6
H' 6000000
H' 600200
H' 600707
H' 6FFFFFF
BUFFER RAM(7)
E7
H' 7000000
H' 7000000
H' 7000FFF
H' 7FFFFFF
INTEGRATED SRAM(35)
VCT1
VCT2
VCT3
VECTOR TABLE 340
PGM3
PGM2
341
PGM1
70

FIG. 6

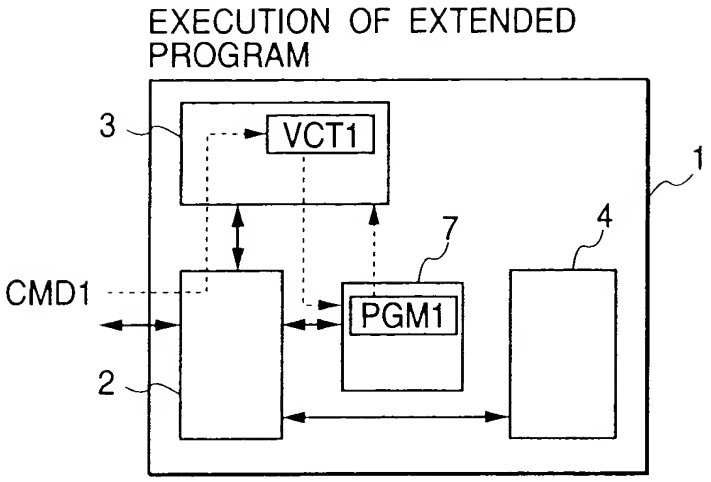
EXECUTION OF EXTENDED PROGRAM
3
VCT1
1
7
4
CMD1
PGM1
2

FIG. 7

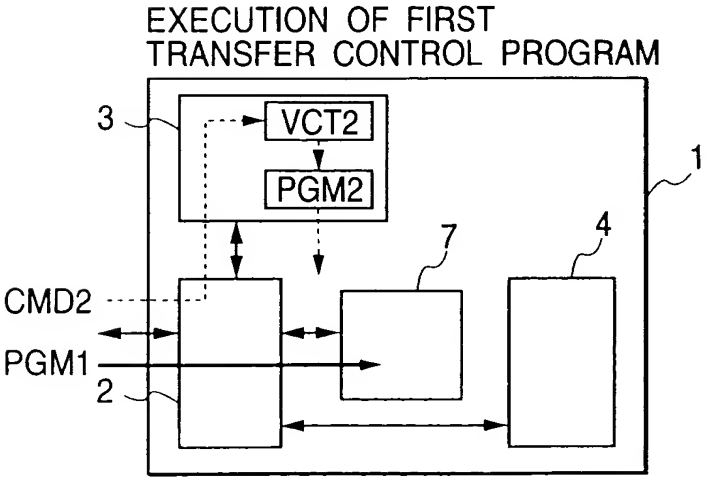
EXECUTION OF FIRST TRANSFER CONTROL PROGRAM
3
VCT2
PGM2
1
7
4
CMD2
PGM1
2

FIG. 8

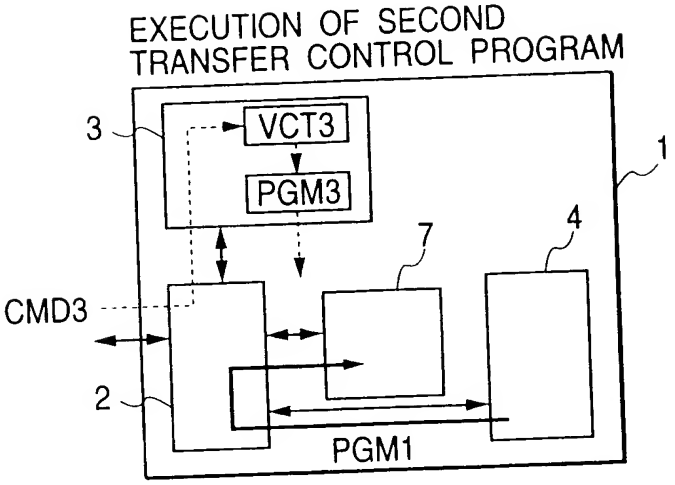
EXECUTION OF SECOND
TRANSFER CONTROL PROGRAM
3
VCT3
PGM3
1
7
4
CMD3
2
PGM1

FIG. 9

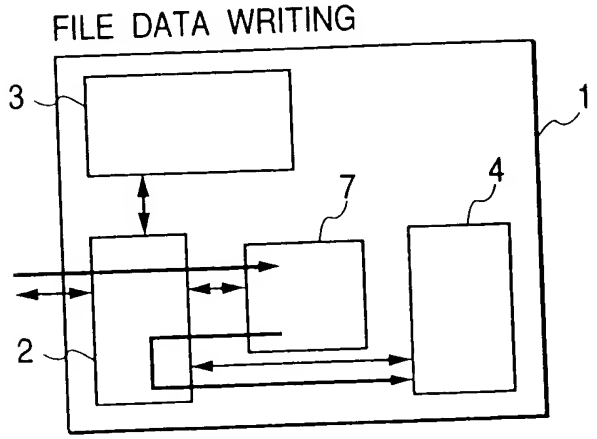
FILE DATA WRITING
3
1
7
4
2

FIG. 10

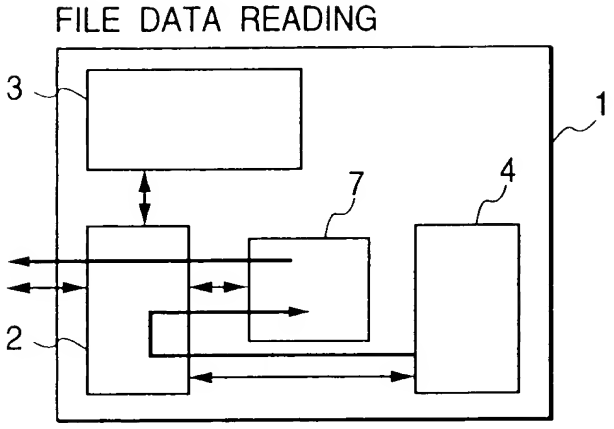
FILE DATA READING
3
1
7
4
2

FIG. 11

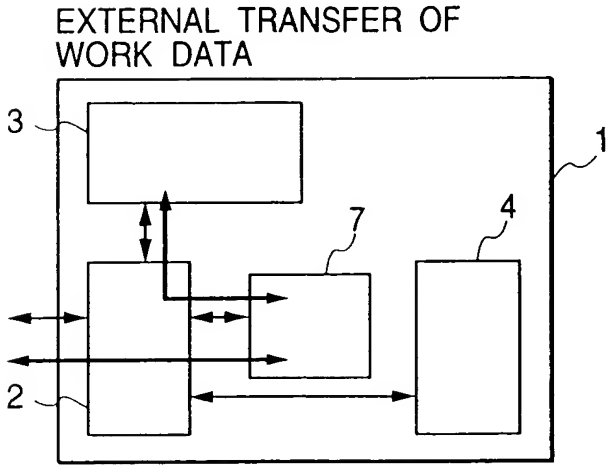
EXTERNAL TRANSFER OF
WORK DATA
3
1
7
4
2

FIG. 12

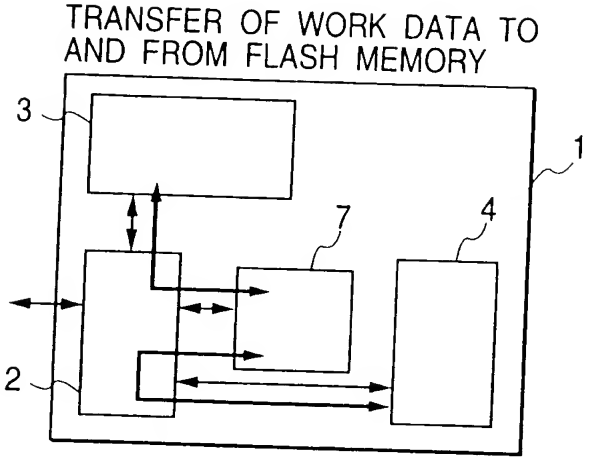
TRANSFER OF WORK DATA TO
AND FROM FLASH MEMORY
3
1
7
4
2

FIG. 14

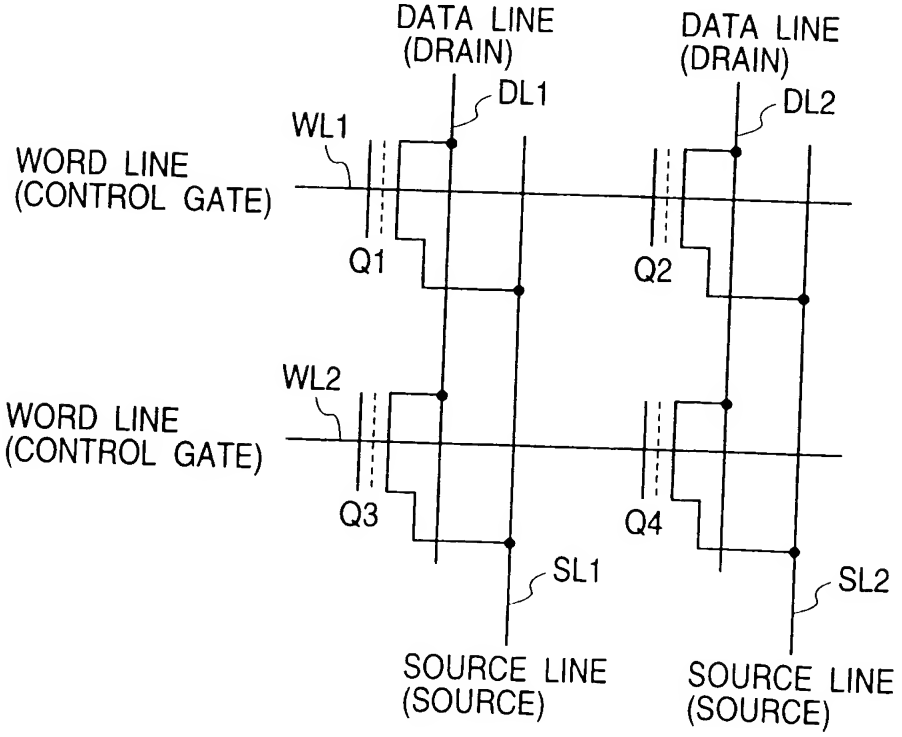
DATA LINE
(DRAIN)
DL1
DATA LINE
(DRAIN)
DL2
WL1
WORD LINE
(CONTROL GATE)
Q1
Q2
WL2
WORD LINE
(CONTROL GATE)
Q3
Q4
SL1
SL2
SOURCE LINE
(SOURCE)
SOURCE LINE
(SOURCE)

FIG. 13(A)

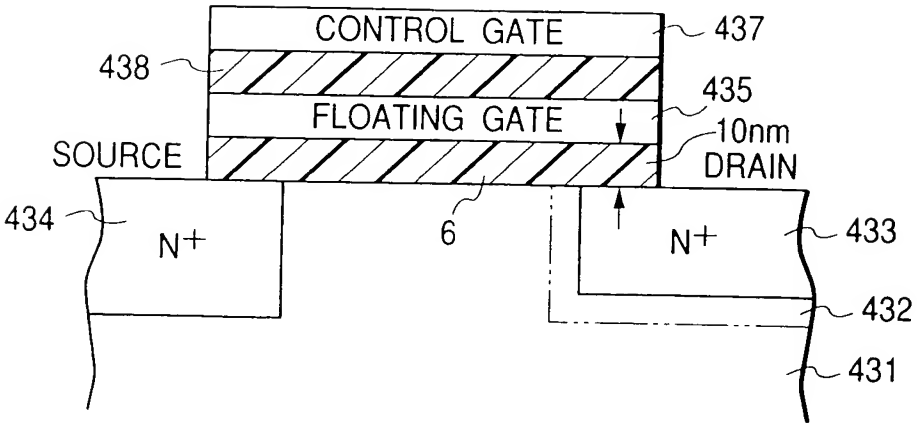

FIG. 13(B)

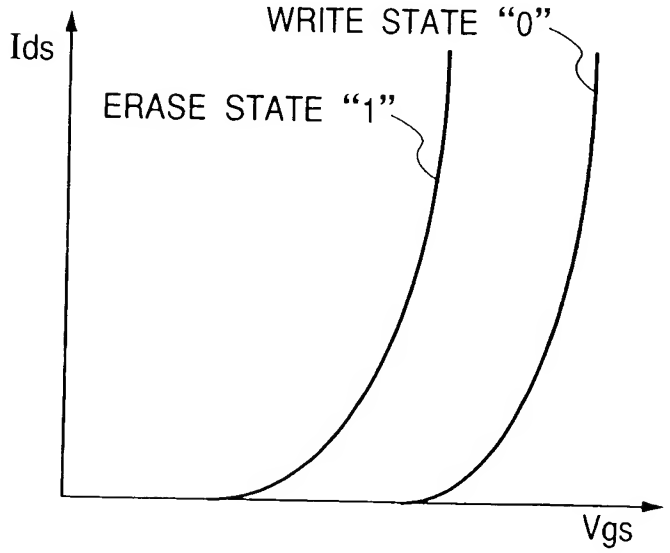

FIG. 15(A)

PROGRAM

MEMORY CELL	SELECTED/ UNSELECTED	SOURCE	DRAIN	CONTROL GATE
Q1	SELECTED	0V	6V	12V
Q2	UNSELECTED	0V	0V	12V
Q3	UNSELECTED	0V	6V	0V
Q4	UNSELECTED	0V	0V	0V

FIG. 15(B)

ERASE (POSITIVE VOLTAGE TYPE)

MEMORY CELL	SELECTED/ UNSELECTED	SOURCE	DRAIN	CONTROL GATE
Q1,Q3	SELECTED	12V	0V	0V
Q2,Q4	UNSELECTED	0V	0V	0V

FIG. 15(C)

ERASE (NEGATIVE VOLTAGE TYPE)

MEMORY CELL	SELECTED/ UNSELECTED	SOURCE	DRAIN	CONTROL GATE
Q1,Q2	SELECTED	5V	0V	−10V
Q3,Q4	UNSELECTED	5V	0V	0V

FIG. 16

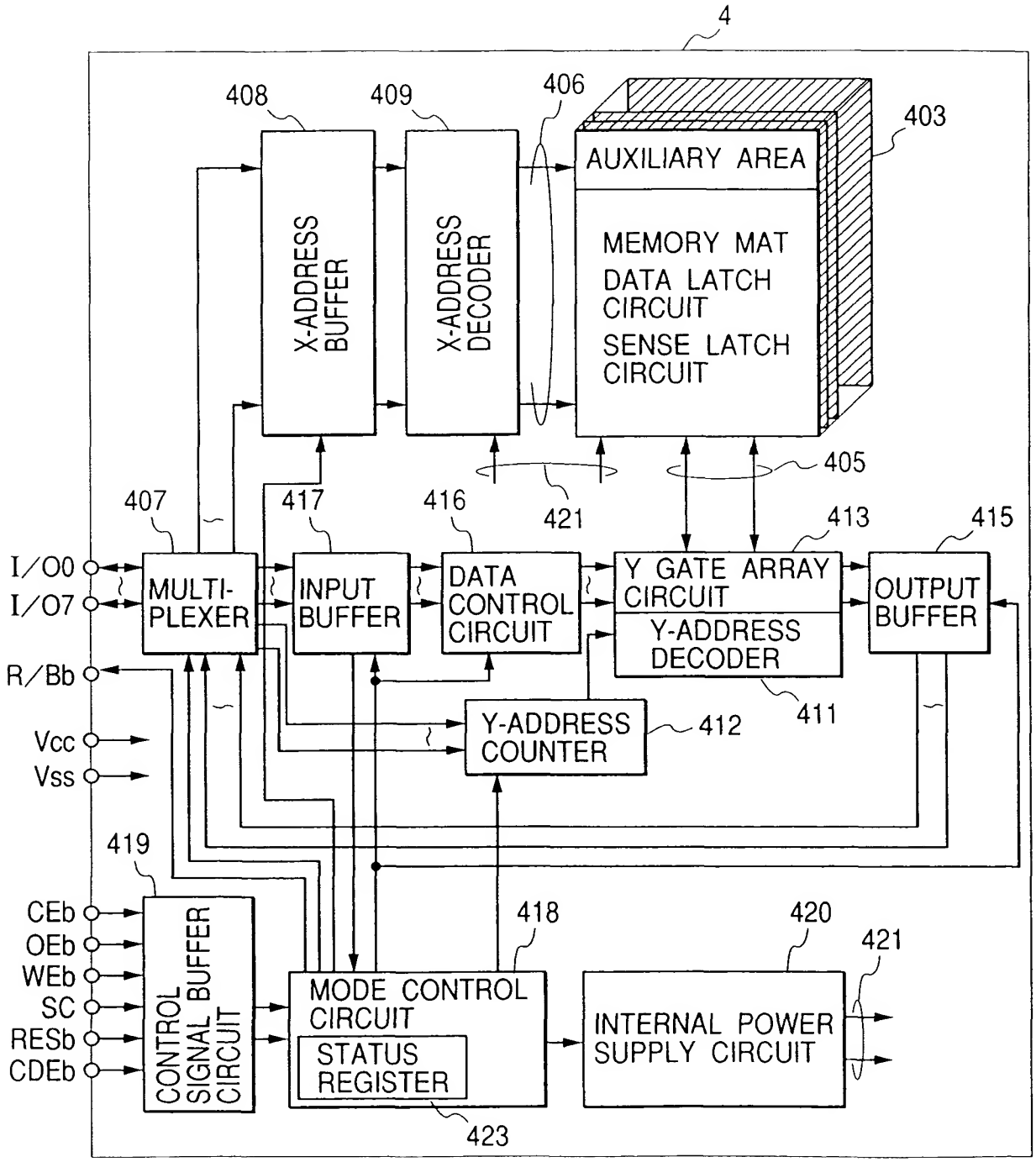
4
408
409
406
403
AUXILIARY AREA
X-ADDRESS BUFFER
X-ADDRESS DECODER
MEMORY MAT
DATA LATCH CIRCUIT
SENSE LATCH CIRCUIT
405
421
407
417
416
413
415
I/O0
I/O7
MULTI-PLEXER
INPUT BUFFER
DATA CONTROL CIRCUIT
Y GATE ARRAY CIRCUIT
Y-ADDRESS DECODER
OUTPUT BUFFER
411
R/Bb
Vcc
Vss
Y-ADDRESS COUNTER
412
419
CEb
OEb
WEb
SC
RESb
CDEb
CONTROL SIGNAL BUFFER CIRCUIT
418
420
421
MODE CONTROL CIRCUIT
STATUS REGISTER
INTERNAL POWER SUPPLY CIRCUIT
423

FIG. 17